INTRODUCTION TO
SOP, SOC, SIP, 3D ICs and 3D Systems

AN INTERDISCIPLINARY ELECTRONIC SYSTEM PERSPECTIVE COURSE
ECE/ME/MSE 6776
FALL 2018

CLASS HOURS	Tuesday / Thursday, 12:00 p.m. – 1:15 p.m. Molecular Science Engineering (MOSE) # MSE 1201A
CREDIT	3 Hours
PREREQUISITES	Introductory packaging course including EE4058 or the consent of an instructor
INSTRUCTOR	Prof. Rao R. Tummala, Petit Chair Professor, ECE and MSE
EXPERT INSTRUCTORS	Prof. G.K. Chang, ECE Prof. Yogendra Joshi, ME Prof. Suresh Sitaraman, ME Prof. Manos Tentzeris, ECE Dr. Sandeep Sane, Intel Dr. Himani Sharma, CHEM Dr. Vanessa Smet, EE Mr. Chris White, ECE
TEACHING ASSISTANT	Mr. Bart Deprospo – bdeprospo@gatech.edu Mr. Grant Spurney – rgspurney@gatech.edu Office Hours: Tuesday, 2:00 p.m. – 3:00 p.m. MaRC 156 (Bart) MaRC 342 (Grant)
PROF. TUMMALA'S ASSISTANT	Ms. Chelsea Heath MaRC 351 chelsea.heath@gatech.edu 404 385-1220
TEXT BOOKS	• "Fundamentals of Microsystems Packaging," McGraw Hill, Tummala, 2001 • "Introduction to System-On-Package (SOP), McGraw-Hill," Tummala and Swaminathan, 2008
COURSE OVERVIEW	This is a system level overview and a cross-disciplinary microsystems packaging course that introduces the new and advanced systems packaging technology concepts that have been explored and developed during the last decade for highly-miniaturized convergent electronic and bio-electronic systems for smart consumer, computer, telecom, wireless, healthcare and automotive systems. The course integrates various disciplines including electrical, materials, chemical, mechanical and bio- engineering to form the basis of new concepts that include SOP, SIP, 3DICs and 3D Systems. Within SOP and 3D Systems, it introduces digital, RF, optical and thermal SOP technologies. This course is intended for graduate students in ECE, ME, MSE, ChemE, Physics and Chemistry. It provides both fundamental and applied aspects of digital and bio-convergent system technologies based on 15 years of intense research advances at the Microsystems Packaging Research Center at Georgia Tech by 35 faculty, 500 graduate students and more than 100 electronic companies. This course will be taught by multiple faculty and some industry experts in their area of expertise.
COURSE FORMAT	1. Lectures

	2. Invited Presentations 3. Student Team Term Papers
COURSE OBJECTIVES	• Provide a system level perspective with an overview of all system technologies and their applications. • Explain what is meant by SOP, SOC, SOB, SIP, MCM, 3D ICs with TSV and 3D System Package. • Explain why and how miniaturize components and systems. • Explain three integration approaches: On-chip, On-package and on-board by transistor scaling, package scaling and systems scaling. • Explain, compare and contrast the 7 key micro-electronic integration technologies: SOB, SOC, MCM, SIP, 3D, SOP, and 3D Systems. • Explain the implications of SOP and 3D technologies for digital convergence. • Explain the role of such disciplines as ECE, ME, ChE, MSE in SOP-based electronics R&D & Manufacturing, as well as in job careers in the industry. • Review all critical SOP technologies: electrical, mechanical and thermal designs, devices, substrate, passive and interconnection materials and processes. • Review allocation of packaging technologies in computing, communication, consumer and in new era of self-driving and electric cars. • Prepare students for industry culture by team work, interdisciplinary, selection of an R&D topic to write and present a term paper with individual contributions
GRADING	• Short quiz: 10% • Mid-term exam: 25% including specific problems • One page summary of 2 chapters: 20% • Attendance: 10% • Final exam: 35% o Individual oral presentation: 15% o Term paper: 20%

Fall 2017 6776 CLASS SCHEDULE

TUESDAY / THURSDAY, 12:00 P.M. – 1:15 P.M., MOSE #G021

Date	Class Topic	Instructor	Special Notes
August			
Tues – 22	Introduction to 6776 Class, What is Packaging and Why?	Tummala	
Thurs – 24	What is SOP and What are SOP Technologies	Tummala	
Tues – 29	Three Types of Packaging and Their Value-add	Tummala	
Thurs – 31	Design: Electrical • Package Electrical Design	Peterson	
September			
Tues – 4	Transistor Scaling Vs. System Scaling • SOC, SIP, MCM,3D ICs	Tummala	
Thurs – 6	• SOC – Its Evolution and Its Future	Tummala	
Tues – 11	Design: Thermal • Thermal Design and Technologies	Joshi	Chpt. Summary #1 Due (at beginning of class)
Thurs – 13	Packaging Materials, Processes and Properties	Sharma	
Tues – 18	• Nanopackaging: Materials and Processes	Sharma	In-Class Quiz
Thurs – 20	• High temperature Materials for Automotive and Other Applications	Raj	
Tues – 25	Package Substrates • Ceramic, Organic, Silicon and Glass	Sundaram	
Thurs – 27	Package Integration Approaches • Stacked ICs and Packages (SIP)	Tummala	
October			
Tues – 2	• 3D ICs with TSV	Tummala	
Thurs – 4	RF, 5G and Millimeter-wave • Design for RF, 5G and mm-Wave	Tentzeris	
Tues – 9	**Fall Break – No Class**		
Thurs – 11	Components: RF and Power • RF Materials, Components and Modules	Raj	
Tues – 16	• Power Components and Modules	Raj	Chpt. Summary #2 Due (at beginning of class)
Thurs – 18	3D System Package – A Fundamental Concept	Tummala	
Tues – 23	2.5D Interposers –Glass vs. Si vs. Organic Interposers	Sundaram	
Thurs – 25	Embedded Packaging • Embedded Components: Chip-First, Chip-Last	Sundaram	Midterm Exam Given Out
Tues – 30	Design: Mechanical • Mechanical Design for Reliability	Sitaraman	
November			
Thurs – 1	Optical Electronics	Chang	
Tues – 6	Automotive Electronics For Self-driving Cars • Sensing Electronics	Sundaram	Midterm Exam Due (at beginning of class)
Thurs – 8	Thermo Mechancial Topic	Sandeep Sane	Guest Instructor, Intel

Tues – 13	Automotive Electronics For Self-driving Cars • High-power Electronics for Electric Cars	Smet	
Thurs – 15	Flexible and Wearable Electronics	Raj and Smet	
Tues – 20	Term Paper Topics and Discussion Interconnections and Assembly • Chip-level	Tummala Smet	
Thurs – 22	**Official School Holiday – Thanksgiving – No Class**		
Tues – 27	• Board-level Assembly	Smet	
Thurs – 29	Comparison of System Technologies and Course Wrap-up	Tummala	
December			
Tues – 4	Lab Tours	White	
Thurs – 6	Term Papers Team Presentations	Tummala	MaRC #114
Sun – 9	Term Papers Due – Submit Online	Shahane / May	Submissions close at 12:00 noon

ECE / ME / MSE 6776 INSTRUCTOR BIOGRAPHIES

Prof. Rao Tummala	Professor Rao Tummala holds the Joseph M. Pettit Chair in Electronics Packaging in the School of Electrical and Computer Engineering and holds a joint faculty appointment in the School of Materials Science and Engineering at Georgia Tech. He is also the Founding Director of the first NSF Engineering Research Center (ERC) at GT called the Microsystems Packaging Research Center (PRC) pioneering the Second Law of Electronics (the first being Moore's Law) by his System-On-Package (SOP) vision. The PRC is currently the largest and most comprehensive microsystems packaging research, education and industry collaboration Center involving on the average about 30 graduate students and 15 faculty from ECE, ME, and MSE departments, collaborating with 40 global companies from the U.S., Europe, Japan, Korea, Taiwan and China; He is the father of industry's 1st MCM, LTCC, plasma display and SOP. He was an IBM Fellow, an IEEE Fellow, Member of National Academy of Engineering, and past president of IEEE CPMT and IMAPS Societies. He is also a Georgia Research Alliance Scholar. Dr. Tummala has published 900 technical papers and invented over 100 patents, wrote the first textbook in packaging, *Microelectronics Packaging Handbook*; wrote the 1st undergrad textbook, *Fundamentals of Microsystem Packaging;* and the 1st SOP book, *Introduction to System-on-Package.* Prof. Tummala may be contacted at rao.tummala@ece.gatech.edu.
Prof. G.K. Chang	Professor Chang received his bachelor's degree in physics from National Tsinghua University in Taiwan and his doctoral degree from the University of California, Riverside. Professor Chang expertise is in the areas of optoelectronic devices, high speed integrated circuits, telecommunication switching components and systems, WDM optical networking systems and networks, optical network security, optical label switching and optical interconnect technologies, TDM- and WDM-PONs, and radio-over-fiber technologies for mobile fronthaul in 5G mobile data communications. He has been an active contributor to many IEEE Photonics Society. Optical Society of America (OSA) sponsored journals, conferences, and committees. He is a pioneer and champion of fiber wireless convergence for broadband wireless access networks that provide high bandwidth, high capacity mobile access for ultra-low latency and ultra-reliable Internet applications. Prof. Chang may be contacted at geekung.chang@ece.gatech.edu.
Prof. Yogendra Joshi	Professor Yogendra Joshi holds joint professorship appointments in the George W. Woodruff of Mechanical Engineering the School of Electrical and Computer Engineering at Georgia Tech. He received an MS in Mechanical Engineering from the State University of New York, Buffalo and his PhD in Mechanical Engineering and Applied Mechanics from the University of Pennsylvania. Professor Joshi's research focuses on thermal and fluid flow issues associated with electronic devices, packages and systems. He is the author or co-author of one 175 journal articles and numerous conference papers. He is also involved in developing internet based distance learning programs in thermal management of electronics. Prof. Joshi is a Fellow of the American Society of Mechanical Engineers, and IEEE. Prof. Joshi may be contacted at yogendra.joshi@me.gatech.edu.
Prof. Suresh Sitaraman	Dr. Sitaraman is a Professor in the George W. Woodruff School of Mechanical Engineering at Georgia Tech. His research focus is in the areas of micro- and nano-scale structure fabrication, characterization, physics-based modeling and reliable design. His micro- and nano-scale research focuses on a wide range of application areas such as aerospace and defense, automotive, computers and telecommunications, portable electronics, and medical. In particular, his research is developing micro-scale and nano-scale structures that can be used as compliant packaging interconnects. Dr. Sitaraman's research also aims to understand the long-term reliability of lead-based and lead-free solder interconnects through thermo-mechanical modeling, material microstructure evolution, reliability experiments, and laser moire interferometry. In parallel, Dr. Sitaraman's research focuses on the next-generation integrated substrates that have high-density interconnects and microvias, embedded passives, and optoelectronic waveguides. In particular, Dr. Sitarman's group has done work in material length

	scale effects for microvia reliability, cure kinetics and interlayer dielectric cracking and delamination, reliability modeling and experiments for embedded passives and optical waveguides. Visit www.me.gatech.edu/caspar for more information about his research. Prof. Sitaraman may be contacted at suresh.sitaraman@me.gatech.edu.
Prof. Emmanouil M. Tentzeris	Professor Manos Tentzeris is the Ken Byers Professor in Flexible Electronics in the School of Electrical and Computer Engineering at Georgia Tech. He received the Diploma degree in Electrical Engineering and Computer Science from the National Technical University in Athens, Greece, and his MS and PhD degrees in Electrical Engineering and Computer Science from the University of Michigan, Ann Arbor. Dr. Tentzeris is the Head of the A.T.H.E.N.A. Research Group (20 students and researchers) and has established academic programs in 3D Printed RF electronics and modules, flexible electronics, origami and morphing electromagnetics, Highly Integrated/Multilayer Packaging for RF and Wireless Applications using ceramic and organic flexible materials, paper-based RFID™s and sensors, inkjet-printed electronics, nanostructures for RF, wireless sensors, power scavenging and wireless power transfer, Microwave MEM's, SOP-integrated (UWB, mutliband, conformal) antennas and Adaptive Numerical Electromagnetics (FDTD, MultiResolution Algorithms). Prof. Tentzeris has published more than 600 papers in refereed Journals and Conference Proceedings, 5 books and 25 book chapters and is an IEEE Fellow. Prof. Tentzeris may be contacted at etentze@ece.gatech.edu.
Dr. P.M. Raj	Dr. P. Markondeya Raj is a Senior Research Engineer and Program Manager for the Passives and their Integration with Actives program at the PRC. He received his PhD from Rutgers University in 1999 in ceramic engineering, ME from the Indian Institute of Science, Bangalore and BS from the Indian Institute of Technology, Kanpur (1993). At PRC, he provides leadership in the areas of power-supply component integration on silicon, glass and organic substrates for power conversion and integrity, RF and precision components (antennas, diplexers, matching networks, nonlinear devices), integrated RF and power modules, and high-temperature packaging. He coauthored 280 publications, which include 11 books, 8 patents with others pending. He received more than 20 "Best Paper" awards for his conference and journal publications. He is the co-Chair for the IEEE CPMT Nanopackaging Technical Committee and Past Chair for the CPMT ECTC High-speed Wireless Components Committee. Dr. Raj may be contacted at raj.pulugurtha@ece.gatech.edu.
Dr. Himani Sharma	Dr. Himani Sharma is Research Scientist-II in the Packaging Research Center (PRC) at Georgia Tech. She received her B.S., M.S. and Ph.D. degrees in Chemistry from University of Delhi, India where she also worked as a chemistry lecturer at undergraduate college. She later, worked as a research associate in Electrical Engineering department in Alabama A&M University on NSA-funded project, before joining Georgia Tech as a Postdoctoral Fellow in 2008. Her research focuses on developing materials for next-generation electronics and packaging. More recently she has been developing passive component technologies focused on improved properties, miniaturization and cost compared to discrete components for digital and RF applications. She has authored more than 60 publications in international peer-reviewed journals and conferences. She has co-authored 1 book and at least 3 book-chapters. She has been awarded Best Poster Award for her work on high density capacitors in 2012 IEEE-Electronic Component and Technology conference. Dr. Sharma may be contacted at himani.sharma@ece.gatech.edu.
Dr. Vanessa Smet	Vanessa is a Research Scientist and Program Manager for Interconnections and Assembly Program at the PRC, focusing on ultra-fine pitch first-level interconnections and MEMS packaging. She received her PhD from University of Montpellier 2, France, in 2010 in electrical engineering (reliability assessment of power modules), BS and MS in applied physics from the ENS Cachan & University of Paris XI, France, in 2007 and 2004, respectively. She was a postdoctoral researcher in Tyndall National Institute, Ireland (2010-2012), working on novel high-temperature high-power die-attachment solutions for power chips and µBGA assembly. Her research interests include power electronics, thermomechanical modeling, 3D integration, interconnections, assembly processes (flip-chip, thermo-compression, SLID) and MEMS

	packaging. Her work has been presented and publishes in international conferences and high impact-factor journals. Dr. Smet may be contacted at vanessa.smet@prc.gatech.edu.
Dr. Venky Sundaram	Venky Sundaram is the Associate Director of Industry Programs at PRC, Georgia Tech and also serves as Program Manager for the Glass Package substrate. He has been with the PRC since 1997 focusing on System on a Package (SOP) technology, ultra-high density substrates and systems integration research. He is a globally recognized expert on 3D packaging, substrates and interposers. He is currently serving as the chair of the IEEE CPMT Technical Committee of High Density Substrates, and as the Director of Student Programs on the Executive Council of IMAPS. Venky is a co-founder of Jacket Micro Devices, an RF substrate and module Georgia Tech PRC Spin-off Company acquired by AVX. He received BS in Metallurgical Engineering from IIT Mumbai, and MS and PhD in Materials Science and Engineering from Georgia Tech. He has several US and international patents and has more than 200 publications in the systems packaging technology. Dr. Sundaram may be contacted at vs24@mail.gatech.edu.
Mr. Chris White	Chris White is a process equipment engineer at the PRC, and also provides Packaging Support for the Institute for Electronics and Nanotechnology (IEN). He has been with the PRC since 2009 focusing on Assembly support and Laboratory Infrastructure. He received his BS in Electrical Engineering from Georgia Tech. Mr. White may be contacted at chris.white@ien.gatech.edu.